AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, ~~at least one of said first and~~the second network[[s]] being a storage area network, said system comprising:

a first data port for receiving first input data and first state information from said first network, said first input data being expressed in said first network protocol;

a second data port for receiving second input data and second state information from said second network ~~indicative of a state of a first storage area network selected from said first and second networks~~, said second input data being expressed in said second network protocol;

a first microsequencer system configured to translate said second input data into corresponding data expressed in said first network protocol on the basis of said first state information, the first microsequencer system including ~~at least one microsequencer, said microsequencer system translating said input data into corresponding data expressed in said second network protocol~~one or more microsequencers configured to cooperate in translating said second input data into corresponding data expressed in said first network protocol;

a second microsequencer system configured to translate said first input data into corresponding data expressed in said second network protocol on the basis of said second state information, the second microsequencer system including one or more microsequencers configured to cooperate in translating said first input data into corresponding data expressed in said second network protocol; and

an instruction memory accessible to each of the ~~at least one~~ microsequencers of the first and second microsequencer systems, said instruction memory having a plurality of instruction words, each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different functional units of each ~~at least one~~of the microsequencers to enable the ~~at least one~~ microsequencers to execute a plurality of instructions in a single instruction cycle.

Claim 2 (currently amended): The system of claim 1, wherein said first and second microsequencer systems comprise[[s]] at least one programmable microsequencer.

Claims 3 and 4 (canceled)

Claim 5 (previously presented): The system of claim 1, further comprising:

an instruction-memory pointer for identifying a selected instruction word in said instruction memory.

Claim 6 (currently amended): The system of claim 4, further comprising a translation-memory accessible to ~~the at least one~~each of the microsequencers of said first and second microsequencer systems, said translation-memory having

a translation-memory address, and

a translation-memory element corresponding to said translation-memory address, said translation-memory element including data for causing an instruction-memory pointer to jump to a selected instruction word.

Claim 7 (original): The system of claim 6, wherein said translation-memory element is configured to include an absolute address of said selected instruction word.

Claim 8 (original): The system of claim 6, wherein said translation-memory element is configured to include an offset from a current instruction word to said selected instruction word.

Claim 9 (original): The system of claim 6, further comprising a translation-memory pointer for indirectly causing said instruction-memory pointer to jump to a selected instruction memory address.

Claim 10 (original): The system of claim 9, wherein said translation-memory pointer is configured to identify a selected translation-memory address corresponding to a translation memory element that contains data indicative of said selected instruction-memory address.

Claim 11 (previously presented): The system of claim 4, further comprising a translation-memory having:

a translation-memory address;

a first translation-memory element corresponding to said translation-memory address, said first translation-memory element including data for causing an instruction-memory pointer to jump to a first instruction word;

a second translation-memory element corresponding to said translation-memory address, said second translation-memory element including data for causing said instruction-memory pointer to jump to a second instruction word; and

a selector for selecting said first translation-memory element.

Claim 12 (original): The system of claim 11, wherein said selector comprises a multiplexer having

a first multiplexer input for receiving data indicative of content of said first translation-memory element;

a second multiplexer input for receiving data indicative of content of said second translation-memory element;

an output providing data selected from at least said first multiplexer input and said second multiplexer input; and

a control input for controlling data provided at said output.

Claim 13 (currently amended): The system of claim 1, further comprising an output port in communication with said second microsequencer system for providing said corresponding data to said second network.

Claim 14 (currently amended): The system of claim 1, wherein said first and second data ports and said first and second microsequencer systems are integrated into one integrated circuit.

Claim 15 (currently amended): A system for enabling communication between a first network having a first network protocol and a second network having a second network protocol, said system comprising:

a first input port for receiving input data from said first network;

a second input port for receiving state information associated with said first network;

[[a]]first and second processing elements in communication with said first and second input ports, one of the processing elements for translating input data from said first network protocol to said second network protocol, and the other for translating input data from said second network protocol to said first network protocol;

an instruction memory accessible to said first and second processing elements, said instruction memory having a plurality of instruction words, each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different cooperating functional units of the first and second processing elements to enable the processing elements to execute a plurality of instructions in a single instruction cycle, said plurality of instruction words being selected to translate input data from said first network protocol to said second network protocol or from said second network protocol to said first network protocol; and

an instruction-memory pointer for identifying a selected instruction word in said instruction memory.

Claim 16 (currently amended): The system of claim 15 wherein said first and second processing elements [[is]]are selected from the group consisting of: a microsequencer system having at least one microsequencer; a micro-processor; and an application-specific integrated circuit.

Claims 17-23 (canceled)